Amendments to the Claims

1. (CURRENTLY AMENDED) An active matrix array device ~~(10)~~ comprising:

a plurality of charging conductors ~~(32)~~;

a plurality of addressing conductors ~~(22)~~ crossing the plurality of charging conductors ~~(32)~~ ; and

a plurality of matrix array elements ~~(100)~~, each matrix array element ~~(100)~~ comprising a first switch ~~(110)~~ having a control terminal coupled to an associated addressing conductor ~~(22)~~ and a data terminal coupled to an associated charging conductor ~~(32)~~, each matrix array element ~~(100)~~ further comprising:

a first capacitive device ~~(120)~~ coupled to a further data terminal of the first switch ~~(110)~~;

a second capacitive device ~~(130)~~ coupled to the first capacitive device ~~(120)~~ via a second switch ~~(112)~~ having a control terminal responsive to an enable signal, the second capacitive device ~~(130)~~ having a smaller capacitance than the first capacitive device ~~(120)~~; and

a third switch ~~(114)~~ coupled between the first capacitive device ~~(120)~~ and a potential source, the third switch ~~(114)~~ having a control terminal coupled to the second capacitive device ~~(130)~~.

2. (CURRENTLY AMENDED) An active matrix array ~~(10)~~ device as claimed in claim 1, wherein each matrix array element ~~(100)~~ further comprises a fourth switch ~~(116)~~ coupled between the first capacitive device ~~(120)~~ and the potential source, the fourth switch ~~(116)~~ having a control terminal being responsive to a further enable signal.

3. (CURRENTLY AMENDED) An active matrix array device ~~(10)~~ as claimed in claim 2, wherein the third switch ~~(114)~~ is coupled between the first capacitive device ~~(120)~~ and the fourth switch ~~(116)~~.

4. (CURRENTLY AMENDED) An active matrix array device ~~(10)~~ as claimed in claim 2, wherein the fourth switch ~~(116)~~ is coupled between the first capacitive device ~~(120)~~ and the third switch ~~(114)~~.

5. (CURRENTLY AMENDED) An active matrix array device ~~(10)~~ as claimed in ~~claim 3 or 4~~claim 3, wherein the second capacitive device ~~(130)~~ comprises a first sub-device (132) and a second sub-device ~~(134)~~, the first sub-device ~~(132)~~ having a first terminal coupled to an enable conductor ~~(42)~~ for providing the enable signal and a second terminal coupled to a data terminal of the second switch ~~(112)~~, the second sub-device having a first terminal coupled to the data terminal of the second switch ~~(112)~~ and a second terminal coupled to a further enable conductor ~~(62)~~ for providing the further enable signal.

6. (CURRENTLY AMENDED) An active matrix array device ~~(10)~~ as claimed in ~~any of the preceding claims~~claim 1, wherein the potential source is provided via the associated charging conductor ~~(32)~~.

7. (CURRENTLY AMENDED) An active matrix array device ~~(10)~~ as claimed in claim 2, wherein each matrix array element ~~(100)~~ further comprises a fifth switch ~~(118)~~ having:

a control terminal responsive to a read-enable signal;

a first data terminal coupled between the third switch ~~(114)~~ and the fourth switch ~~(116)~~; and

a further data terminal coupled to a read-out conductor.

8. (CURRENTLY AMENDED) An active matrix array device ~~(10)~~ as claimed in claim 4, wherein the second switch ~~(112)~~ is of a different channel type than the fourth switch ~~(116)~~, the control terminal of the second switch ~~(112)~~ and the control terminal of the fourth switch ~~(116)~~ being coupled to a common conductor ~~(42)~~.

9. (CURRENTLY AMENDED) An electronic device ~~(500)~~ comprising:

an active matrix array device ~~(10)~~ comprising:

a plurality of charging conductors ~~(32)~~;

a plurality of addressing conductors ~~(22)~~ crossing the plurality of charging conductors ~~(32)~~; and

a plurality of matrix array elements ~~(100)~~, each matrix array element ~~(100)~~ comprising a first switch ~~(110)~~ having a control terminal coupled to an associated addressing conductor ~~(22)~~ and a data terminal coupled to an associated charging

conductor ~~(32)~~, each matrix array element ~~(100)~~ further comprising:

a first capacitive device ~~(120)~~ coupled to a further data terminal of the first switch ~~(110)~~;

a second capacitive device ~~(130)~~ coupled to the first capacitive device ~~(120)~~ via a second switch ~~(112)~~ having a control terminal responsive to an enable signal, the second capacitive device ~~(130)~~ having a smaller capacitance than the first capacitive device ~~(120)~~; and

a third switch ~~(114)~~ coupled between the first capacitive device ~~(120)~~ and a potential source, the third switch ~~(114)~~ having a control terminal coupled

to the second capacitive device ~~(130)~~;

the electronic device ~~(500)~~ further comprising:

drive circuitry ~~(20)~~ for driving a plurality of signals onto the plurality of addressing conductors ~~(22)~~;

further drive circuitry ~~(30)~~ for driving a plurality of further signals onto the plurality of addressing conductors ~~(32)~~; and

a power supply ~~(52)~~ for powering the drive circuitry ~~(20)~~ and the further drive circuitry ~~(30)~~.

10. (CURRENTLY AMENDED) A method of operating an active matrix array device ~~(10)~~ having a plurality of matrix array elements ~~(100)~~ including first and second capacitive devices ~~(120; 130)~~, comprising:

storing a first voltage across the first capacitive device ~~(120)~~ of a matrix array element ~~(100)~~;

storing the first voltage across the second capacitive device ~~(130)~~ of the matrix element ~~(100)~~;

replacing the first voltage across the first capacitive device ~~(120)~~ of the matrix array element ~~(100)~~ with a second voltage; and

depending on the magnitude of the first voltage stored across the second capacitive device ~~(130)~~, enabling a current path between the first capacitive device ~~(120)~~ and a potential source for replacing the second voltage across the first capacitive device ~~(120)~~ with a third voltage.